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Design of Low Power Sequential System Using Multi Bit FLIP-FLOP With Data Driven Clock Gating

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ABSTRACT
Power reduction plays a vital role in VLSI design .The Data driven clock gating is used for reduce power consumption in synchronous circuits .Common clock gating is used for power saving. However clock gating still leaves larger amount of redundant clock pulses. Multibit flip-flop is also used to reduce power consumption .Using of Multibit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flip-flop .Combination of Multibit Flip-Flop with Data driven clock gating will increase the further power saving. Xilinx software tool and quatrus II for power analysis is used for implementing this proposed system.

I. Introduction

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power, since it removes large numbers of mixes and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. However, note that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree.

Clock gating logic can be added into a design in a variety of ways:

1. Coded into the RTL code as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating).
2. Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers.
3. Semi-automatically inserted into the RTL by automated clock gating tools. These tools either insert ICG cells into the RTL, or add enable conditions into the RTL code. These typically also offer sequential clock gating optimizations.

II. Literature Survey

Clock power is the major contributor to dynamic power for modern integrated circuit design. A conventional single-bit flip-flop cell uses an inverter chain with a high drive strength to drive the clock signal. Clustering several such cells and forming a multibit flip-flop can share the drive strength, dynamic power, and area of the inverter chain, and can even save the clock network power and facilitate the skew control. Hence, in this paper, we focus on post placement multibit flip-flop clustering to gain these benefits. Utilizing the properties of Manhattan distance and coordinate transformation, we model the problem instance by two interval graphs and use a pair of linear-sized sequences as our representation. Digital System Clocking is assuming ever greater importance as clock speeds increase, doubling every three years. This the first book to focus entirely on clocked storage elements, "Flip-Flops" or Latches"—provides an in-depth introduction to the subject for both professional computer design engineers and graduate-level computer engineering students. In Digital System Clocking: High-Performance and Low-Power Aspects, you will find information on. Our method simultaneously performs (1) activity-aware register clustering that reduces clock tree power not only by clumping registers into a smaller area, but pulling the registers with similar activity pattern close to shut off more time for the resultant sub trees; (2) timing and activity based net weighting that reduce net switching power by assigning a combination of activity and timing weights to the nets with higher switching rates or more critical timing; (3) gate control logic optimization that still set the gate enable signal high if a register is active

for a number of consecutive clock cycles. Experimental results show that our approach is able to reduce the power and total wire length of clock tree greatly with minimal overheads.

III. Existing System

In existing system power reduction is achieved by using clock gating. With clock gating, the Clock signals are multiply with an AND gate logic to explicitly predefined enabling signal. But this clock gating still leaves large number of redundant clock pulses. Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synthesis algorithms, from register transfer level (RTL) down to gate level and net list. Unfortunately, such automation leads to a large number of unnecessary clock toggle, thus increasing the number of wasted clock pulses at flip-flops (FFs) as shown in this paper through several industrial examples. Consequently, development of automatic and effective methods to reduce this inefficiency is desirable. In the sequel, we will use the terms toggling, switching, and activity interchangeably.

IV. Proposed System

Multi-bit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flip-flops. Data driven clock gating reduce redundant clock pulses. Combination of Multi-bit Flip-Flop with Data driven clock gating will increase the further power saving. Xilinx software tool is used for implementing this proposed system. This paper studies data-driven clock gating, employed for FFs at the gate level, which is the most aggressive possible. The clock signal driving a FF is disabled (gated) when the FFs state is not subject to change in the next clock cycle [7]. Data-driven gating is causing area and power overheads that must be considered. In an attempt to reduce the overhead, it is proposed to group several FFs to be driven by the same clock signal, generated by bring the enabling signals of the individual FFs. This may however, lower the disabling effectiveness. It is therefore beneficial to group FFs whose switching activities are highly correlated and derive a joint enabling signal. In a recent paper, a model for data-driven gating is developed based on the toggling activity of the constituent FFs [9]. The optimal fan-out of a clock gater yielding maximal power savings is derived based on the average toggling statistics of the individual FFs, process technology, and cell library in use. In general, the state transitions of FFs in digital systems depend on the data they process. Assessing the effectiveness of data-driven clock gating requires, therefore, extensive simulations and statistical analysis of the FFs' activity. Another grouping of FFs for clock switching power reduction, called multi-bit FF (MBFF), has recently been proposed in [10] and [11]. MBFF attempts to physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs in a group. MBFF grouping is mainly driven by the physical position proximity of individual FFs, while grouping for data-driven clock gating should combine toggling similarity with physical position considerations. While [9] answered the question of what is the group size that maximizes power savings, this paper studies the questions of: 1) which FFs should be placed in a group to maximize the power reduction and 2) how to algorithmically derive those groups. We also describe a backend design flow implementation.

4.1 Data-Driven Clock Gating

Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every FF as a part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions of their underlying FFs depend on the data being processed. It is important to note that the entire dynamic power consumed by a system stems from the periods where modules' clock signals are enabled. Therefore, regardless of how relatively small this period is, assessing the effectiveness of clock gating requires extensive simulations and statistical analysis of FFs toggling activity, as presented subsequently.

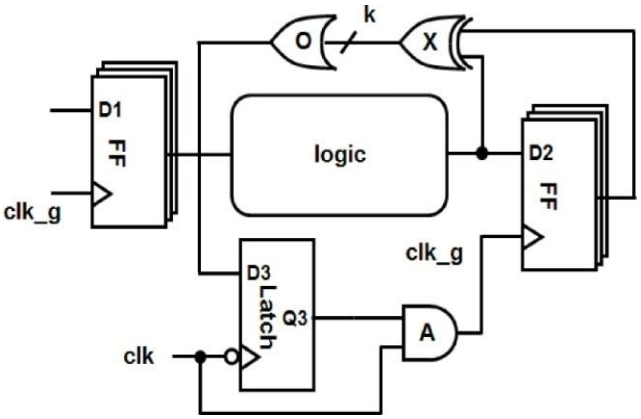


Fig. 1 Practical data-driven clock gating.

The latch and gater (AND gate) overheads are amortized over *k* FFs.

Let the average toggling probability of a FF (also called activity factor) be denoted by p ($0 < p < 1$). Under the worst-case assumption of independent FF toggling, and assuming a uniform physical clock tree structure, it is shown in [9] that the number k of

jointly gated FFs for which the power savings are maximized is the solution of

$$(1-p)^k \ln(1-p)\,(c_{FF}+c_W) + c_{latch}/k^2 = 0 \qquad (1)$$

Where c_{FF} is the FFs clock input capacitance, c_W is the unit-size wire capacitance, and c_{latch} is the latch capacitance including the wire capacitance of its *clk* input. Table I shows how the optimal k depends on p. Such a gating scheme has considerable timing implications, which are discussed in [9]. We will return to those when discussing the implementation of data-driven gating as a part of a complete design flow.

4.2 Implementation and Integration Ina Design Flow

In the following, we describe the implementation of data-driven clock gating as a part of a standard backend design flow. It consists of the following steps.

1) Estimating the FFs toggling probabilities involves running an extensive test bench representing typical operation modes of the system to determine the size k of a gated FF group by solving (1).
2) Running the placement tool in hand to get preliminary preferred locations of FFs in the layout.
3) Employing a FFs grouping tool to implement the model and algorithms presented in Sections III and IV, using the toggling correlation data obtained in Step 1 and FF locations' data obtained in Step 2. The outcome of this step is k-size FF sets (with manual overrides if required), where the FFs in each set will be jointly clocked by a common gater.
4) Introducing the data-driven clock gating logic into the hardware description (we use Verilog HDL). This is done automatically by a software tool, adding appropriate Verilog code to implement the logic described in Fig. 2. The FFs are connected according to the grouping obtained in Step 3. A delicate practical question is whether to introduce the gating logic into RTL or gate-level description. This depends on design methodology in use and its discussion is beyond the scope of this paper. We have introduced the gating logic into the RTL description.
5) Re-running the test bench of Step 1 to verify the full identity of FFs' outputs before and after the introduction of gating logic. Although data-driven gating, by its very definition, should not change the logic of signals, and hence FFs toggling should stay identical, a robust design flow must implement this step.
6) Ordinary backend flow completion. From this point, the backend design flow proceeds by applying ordinary place and route tools. This is followed by running clock-tree synthesis.

V. Simulation Results

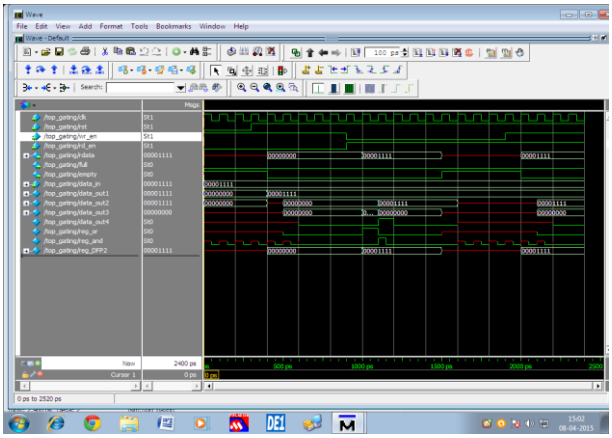


Fig. 2 Output Waveform of Clock Gated Synchronous FIFO

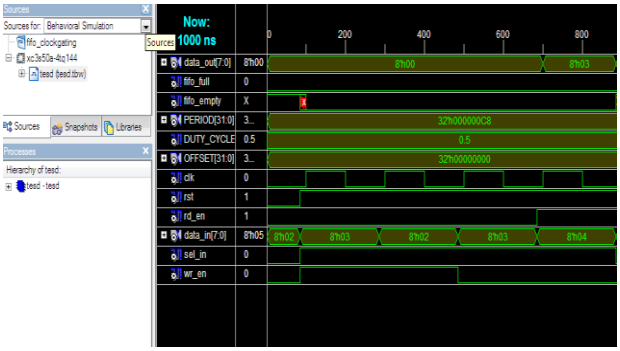
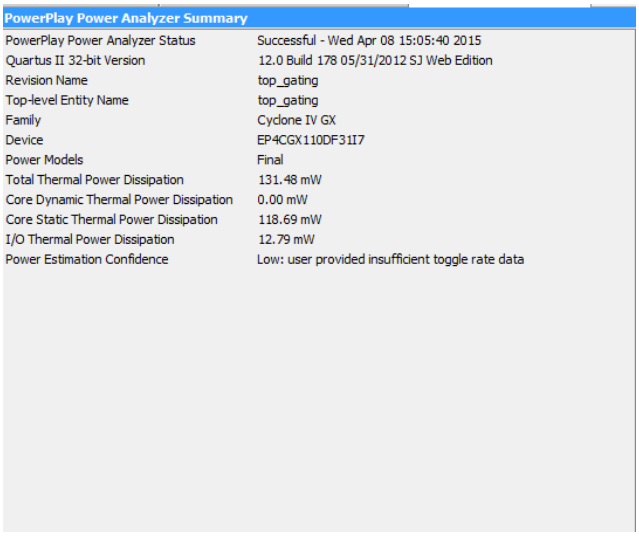


Fig. 3 Output Wave form of Synchronous FIFO Using Multibit Flipflop With Data Driven Clock Gating.



PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Wed Apr 08 15:05:40 2015
Quartus II 32-bit Version	12.0 Build 178 05/31/2012 SJ Web Edition
Revision Name	top_gating
Top-level Entity Name	top_gating
Family	Cyclone IV GX
Device	EP4CGX110DF31I7
Power Models	Final
Total Thermal Power Dissipation	131.48 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	118.69 mW
I/O Thermal Power Dissipation	12.79 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig .4 Power Analyzer Summary

Clock gating is used in fifo to reduce the power consumption. For further power saving data driven clock gating and multi-bit flip-flops are used in sequential circuits. Common clock gating is used for power saving. But clock gating still leaves larger amount of redundant clock pulses. Multi-bit flip-flop is also used to reduce power consumption. Using of Multi-bit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flip-flops.

VI. Conclusion

Clock gating is used in fifo to reduce the power consumption. For further power saving data driven clock gating and multibit flip-flops are used in sequential circuits. Common clock gating is used for power saving. But clock gating still leaves larger amount of redundant clock pulses. Multibit flip-flop is also used to reduce power consumption. Using of Multibit Flip-Flop method is to eliminate the total inverter number by sharing the inverters in the flip-flops. Combination of Multibit Flip-Flop with Data driven clock gating will increase the further power saving. Xilinx software tool is used for implementing this proposed system. The combination of data-driven gating with MBFF in an attempt to yield further power savings.

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